IMP-HOST INTERFACE FLOW DIAGRAMS

The following flow diagrams were extracted from the logic diagrams provided in Appendix B of BEN Report No. 1822. These diagrams indicate the logical sequence of hardware operations which occur within the IMP-HOST interface. The logic names appearing in the blocks correspond to the logic elements found in Appendix B.
IMP to HOST Message

Start
Input

LAST ← 0; IMPERR ← 0
PAD ← 0; IN REST ← 0
COUNTER ← 0

RFNIB ← 1

Theres
Your bit
-1?

Y

IMP ERROR ← 1

IMP READY ← 2

Y

LAST
IMP BIT ← 1

N

PAD ← 1

Pulse shift reg.
Increment counter
RFNIB ← 4 ← 0

B

C

A
START OUTPUT

COUNTER ← 1
LSTWD ← 0; BTAVL ← 0

OUT REQST ← 1
CLEAR SHIFT REG.

STROBE
DATA WORD = 1?

Y

LOAD SHIFT REGISTER
OUT REQST ← 0
COUNTER ← 1

N

RENBIT = 1/2?

Y

THERE'S YOUR HOST BIT ← 1

N

RENBIT = 0?

Y

A

C

B